REMARKS

This Amendment under Rule 116 is filed in response to the FINAL Office Action mailed on March 10, 2005. All objections and rejections are respectfully traversed.

Claims 1-48 are in the case.

Claims 30 and 39 were amended to better claim the invention..

No claims were added.

At Paragraphs 1-13 of the Office Action, Claims 1, 2, 4-7, 11-16, 18 and 21-23, 25-28, 31, 32, 34-37, 40, 41, 43 and 44 were rejected under 35 U.S.C. 102(e) as being anticipated by Wu U. S. Patent No. 6,151,644 issued on November 21, 2000 (hereinafter Wu).

The present invention, as set forth in representative claim 1, comprises in part:

1. A method for ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers***, the method comprising the steps of:
including a context memory in each pipeline row;

organizing the context memory as a plurality of window buffers of a defined size;

apportioning each packet into contexts corresponding to the defined size associated with each window buffer; and

correlating each context with a relative position within the packet to thereby facilitate reassembly of the packet at the output buffer, while obviating out of order issues involving the contexts of the packet.

Wu discloses a dynamically configurable buffer for a device for a computer network. Wu's buffer is first configured for a large size "packet buffer", and also is configured with a packet buffer divided into smaller pieces referred to as a "packet cell". A large packet is stored in a "packet buffer", and a small packet may be stored in a "packet cell" if the packet is small enough. The packet cell size can be increased dynamically to accommodate different size packets.

Wu has a Memory Arbitrator 24 between a Receive Module 20 and a Transmit Module 22. The Wu Receive Module 20 is shown in Wu's Fig. 4 as receiving incoming packets at Network Interface 66, and outputting data at module 67, and outputting address at module 68. Wu's transmit module 22 is shown in Wu's Fig. 10, where his packets are transmitted on line 14 to the next network (Wu Fig. 1, Fig. 2, Fig. 10).

Applicant respectfully urges that Wu has no disclosure of Applicant's claimed novel ***striping packets across pipelines of a processing engine within a network switch,***

the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output buffers. Particularly, Wu has no disclosure of Applicant's claimed ***plurality of processors arrayed as pipeline rows and columns***.

Applicant further urges that Wu is silent concerning Applicant's claimed novel ***pipelines of a processing engine.*** That is, Wu has no disclosure of Applicant's claimed ***pipelines***.

Also, Applicant respectfully urges that Wu has no disclosure of Applicant's claimed novel ***including a context memory in each pipeline row***. Firstly, Wu has no disclosure of Applicant's claimed ***each pipeline row***. Secondly Wu has no disclosure of Applicant's claimed novel ***including a context memory*** in his design. Further, Wu has no disclosure of ***including a context memory in each pipeline row***, especially since Wu has no disclosure of a ***pipeline row***.

Accordingly, Applicant respectfully urges that Wu is legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. § 102 because of the absence from Wu of Applicants claimed novel ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns embedded between input and output***

buffers; and there is absent from Wu Applicant's claimed novel ***plurality of processors arrayed as pipeline rows and columns***.

At Paragraphs 14-17 of the Office Action Claims 3, 8, 17, 19, 24, 29, 33, 38, 42, 47, and 48 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Sindhu.

Applicant respectfully notes that Claims 3, 8, 17, 19, 24, 29, 33, 38, 42, 47, and 48 are dependent from independent claims, and the independent claims are believed to be in condition for allowance. Accordingly, Claims 3, 8, 17, 19, 24, 29, 33, 38, 42, 47, and 48 are believed to be in condition for allowance.

At Paragraph 18 of the Office Action, Claims 9, 10, and 20 were allowed.

At Paragraph 19 of the Office Action Claims 30 and 39 were indicated to be allowable if written in independent form. Amendment of the Claims 30 and 39 is believed to satisfy this requirement.

At Paragraph 20 of the Office Action, The Examiner Responded to Applicant's arguments.

The Examiner stated:

> "Wu teaches the processing engine having a plurality of processors arrayed as pipeline rows and columns (fig. 3a-sF) embedded between input (20) and output buffers (fig. 2)."

However, Wu states at his Column 4 Line 35 through Column 7 Line 7:

> "Receive module 20 stores the five packets P1-P5 in buffer memory 18 as they arrive. . . .After storing large packet P1 in packet buffer PB0, receive module 20 stores the next packet (P2) in the first cell C0 of the next unoccupied packet buffer PB1. . . .Receive module 20 will continue to write incoming packets arriving after packet OB5 to the remaining packet buffer PB2-PBN in a similar manner until all packet buffers PB0-PBN have received either a single large packet or a sequence of one or more small packets. . . . Receive module 20 then resets WRITE_CELL_PTR to 0 and loads LOOKAHEAD_PTR into register 26 so that it will be ready to begin storing a next incoming packet in buffer PB3."

That is, Wu gives a detailed description of storing packets into his packet buffers. However, Applicant respectfully urges that Wu is completely silent concerning Applicant's claimed novel ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns.***

Further, Wu is silent concerning Applicant's claimed ***the processing engine having a plurality of processors arrayed as pipeline rows and columns.***

Because Wu is silent concerning Applicant's claimed novel ***striping packets across pipelines of a processing engine within a network switch, the processing engine having a plurality of processors arrayed as pipeline rows and columns***, Applicant respectfully urges that Wu is legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. § 102.

All independent claims are believed to be in condition for allowance.

All dependent claims are dependent from independent claims which are believed to be in condition for allowance. Accordingly, all dependent claims are believed to be in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

A. Sidney Johnston
Reg. No. 29,548
CESARI AND MCKENNA, LLP
88 Black Falcon Avenue
Boston, MA 02210-2414
(617) 951-2500